Are Smart Cards the Ideal Domain for Applying Formal Methods ?

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1 Introduction

The traditional approach for programming smart cards does not allow the creation of downloadable executable code and requires programmers with experience in programming in low-level languages. This approach, associated with a high quality qualification process, produce secured smart card. Unfortunately, it does not allow card manufacturers and issuers to quickly respond to the market changes, and it limits the flexibility of smart card applications. Open smart card programming provides a more dynamic approach to card applications. High-level languages and security mechanisms are the basis for the programming of open smart cards. Most notable efforts towards such smart card systems are Java Card [22], MultOS [14] and Smart Card for Windows [15], which provide application developers an opportunity to develop rapidly applications. The main drawback with this kind of smart card is the risk to download a hostile application that will exploit a faulty implementation module of the platform.Security is always a big concern for smart cards, but the issue is getting more intense with multi-applicative platforms and post issuance code downloading. The correct design and implementation of the system is the key to shun such an attack. Fault prevention offers different techniques to remove latent errors from the system. The fault avoidance concerns methodologies and appropriate techniques to avoid the introduction of fault during the design and the construction of the system. In a first approach, one can believe that smart card can only get benefits of using formal methods. But it remains difficult to integrate these methods in the development process.

The need of formal methods in the smart card domain has three origins: mastering the complexity of the new operating systems (fault avoidance), certifying at a high level a part of the smart card and reducing the cost of the test. In a first part, after presenting the smart card and its security requirements, we explain the certification process that appears to be the most important vector for introducing formal methods in the software development cycle. Then we present some attempts to formalise complex software elements of smart cards. The use of model checkers in order to automatically generate the test suites can notably increase the productivity of applet development. The second part of this paper explains why smart cards are not currently the expected success story of formal methods.

2 Needs of security and formalism

2.1 The small and secure system

A smart card is a piece of plastic, the size of a credit card, in which a single chip microcontroller is embedded. Usually, microcontrollers for cards contain a microprocessor (8-bit ones are the most widespread, but 16-bit and 32-bit processors can now be embedded in the chip) and different kinds of memories: RAM (for run-time data), ROM (in which the operating system and the basic applications are stored), and EEPROM (in which the persistent data are stored). Since there are strong size constraints on the chip, the amounts of memory are small. Most smart cards sold today embed a chip with at most 512 bytes of RAM, 32 KB of ROM, and 16 KB of EEPROM. Today's smart card devices have no on-chip power and no clock. This means that the security functions are limited and cannot presume about the reliability of clock or power. The chip usually also implements some techniques and functions in order to safeguard information like limit sensors (heat, voltage, clock *etc.*), scrambled and distributed layout, data encryption and memory segregation which are used to deactivate the card when it's somehow physically attacked. A smart card cannot be totally secure; it must just be secure enough, the goal is to make it sufficiently tamper-resistant.

Smart cards are not only storage media; they are able to execute application software with cryptographic functions (DES, triple DES, RSA, DSS or elliptic curves). It makes them a key technology for numerous high-security consumer applications. Smart cards are often used either to store or manage some kind of currency (money or tokens), to record personal information (like medical history), or to identify a person. In these applications, smart cards provide a means to guarantee the security (confidentiality and integrity) of the whole system. In fact, a failure of a smart card impacts the reliability of the system. With open smart cards, functionality of the card can be extended by downloading new programs into the card. The security requirements for such an operating system are more stringent than those for conventional cards. The ability of adding new applications after the issuance poses a threat and particular attention must be paid to the post issuance loading or deleting of application.

The cardholder or a hacker has a complete control over the card after issuance and can subject it to any number of hacking attempts. For these reasons (high value object, physical and logical attack in a discrete environment without any on-line detection mechanism) the smart card is often the target of hackers. Since around 1994, some smart cards used in pay-TV have been successfully reverse engineered. Most of the attacks were carried out without any access to information from the manufacturer.

In order to reach the smart cards quality requirements, it is of prime importance to eradicate all the latent errors in the smart card software. For this reason, the card issuer must develop a test strategy that eliminates all the errors or use new development techniques. Formal methods for specification and verification have always been among the central issues in computer science. It has a considerable impact in the hardware industry but its impact on the software development process has been limited. This is due to the complexity of modern software system involving thousand of lines of code. The smart card operating system and the embedded applications are relatively small. They are well within the limits of what can be handled by modern verification tools. Several attempts to formalize part of smart card operating systems or applications have been done by academic researchers. Some similar work is probably done by smart card providers but a few papers have been published.

2.2 The certification process

As we saw, the security is the main characteristic of smart cards. Each smart card provider claims that its product has the *ad-hoc* security. This claim can be enforced by submitting the product for certification by an independent evaluation lab. This process is a means to gain market share by highlighting the differences between smart card providers. Sometimes regulation requires the use of certified product for some markets. Currently, a certification at an EAL4 level is mandatory in Germany and Hungary for systems that use private signature keys.

The Common Criteria for Information Technology Security Evaluation (CC) standard defines a set of criteria to evaluate the security properties of a product in term of confidentiality, integrity and availability. The framework is being developed jointly by the IEC (International Electrotechnical Commission) and ISO (International Standards Organisation), with the participation of national bodies. It is drawn from previous security requirements and assurance frameworks that are the ITSEC and TCSEC.

The CC focuses mainly on the first part of the lifecycle: requirements, specifications, design, development and test. The deployment and the maintenance are not covered by the CC. The requirement phase is the most important part. The CC are used for writing the requirements document which must be complemented by a general requirement document because the CC are only concerned by the security aspects of the system.

The Target Of Evaluation (TOE) is the part of the product or the system that is subject to evaluation. The TOE security threats, objectives, requirements, and summary specification of security functions and assurances measures together form the primary inputs to the Security Target (ST). It's used by the evaluators as the basis for evaluation. The CC also defines the Protection Profile (PP) that allows the developers to create sets of security requirements available for several TOEs. A PP is intended to be reusable. The CC presents the security requirements under the distinct categories of functional requirements (*e.g.*, requirements for identification, authentication, non-repudiation) and assurance requirements (*e.g.*, constraints on the development process rigour, impacts of potential security vulnerabilities). The assurance that the security objectives are achieved is linked to:

– The confidence in the correctness of the security functions implementation, *i.e.*, the assessment whether they are correctly implemented,
– The confidence in the effectiveness of the security functions, *i.e.*, the assessment whether they actually satisfy the stated security objectives.

The CC contains a set of defined assurance levels that define a scale for measuring the criteria for the evaluation of PPs and STs. The Evaluation Assurance Levels (EAL1 to EAL7) form an ordered set to allow simple comparison between TOEs of the same kind. The role of the EALS is the same as the ITSEC security levels, although they represent only assurance requirements. EAL levels may be augmented to include higher assurance requirements or to substitute assurance components. Note that the EAL may only be augmented. At EAL5 level the assurance is gained through a **formal** model of the TOE **security policy** and a **semiformal** presentation of the functional specification and high-level design and a **semiformal** demonstration of *correspondence* between them. A modular TOE is also required. Note that the analysis must include validation of the developers covert channel analysis. The last EAL levels require a formal in-depth and exhaustive analysis.

Three types of specification styles are mandated by the CC: informal, semiformal and formal. An informal specification is written in natural language and is not subject to any notational restriction but it requires defining the meanings of the used terms. A **semiformal** notation is written with a restricted syntax language and may be diagrammatic (data-flow diagrams, state transition diagrams, entity-relationship diagrams, *etc*). A **formal** description is written in a notation based upon well-established mathematical concepts. These concepts define the syntax and the semantics of the notation and the proof rules that support logical reasoning. A *correspondence* can take the form of an informal demonstration, a **semiformal** demonstration or a **formal** proof. A semiformal demonstration of correspondence requires a structured approach at the analysis of the *correspondence*. A formal proof requires well-established mathematical concepts and the ability to express the security properties in the formal specification language.

It is important to notice that in the USA a complete scheme for certification is set up. Seven labs received accreditation for evaluation. This year in Baltimore will be held the first "Common Criteria Conference". At the beginning of the year the SCSUG (Smart Card Security User Group) specified a new PP for open operating systems like Java Card, Windows for Smart Cards and Multos. This shows clearly the involvement of the USA to fill the gap between them and Europeans country and the importance of the certification process.

Gemplus obtained the first common criteria for Java Card last year. Two others certificates EAL4+ are forecast for this summer and other certifications are planned. The smart card dedicated protection profiles (PP) were defined in 1999 for EAL4 certification. This year several PP have been published in order to reach EAL5 certification. Moreover the GIE Carte Bancaire that requested EAL3+ certificate is now moving to at least an EAL5 level. Multos obtained in 1999 the first ITSEC E6 certificate for a part of its operating system. This demonstrates that customers are requiring higher level certificates.

2.3 The complexity is increasing

Until now the complexity of smart card software was manageable by engineers. The size of a smart card application was around some thousand of C code lines and they all had quite the same architecture. The arrival of Java brings to the fore the complexity of the underlying mechanisms used in the virtual machine. It is not surprising if the first formal model of smart cards where devoted to this architecture. Java Card is a subset of Java that reduces the complexity of the model. This is probably the reason of the success of the formal specification of Java Card components. A lot of work has been done in the smart card domain but unfortunately no one achieved a proof of a complete smart card application neither a complete component of the virtual machine. There have been several efforts to formalise components of smart cards:

In [2], the authors present a part of a stack-based interpreter for a smart card based system: Tosca. The interpreter is object-based and is written in Clasp. It shares several features with Forth (*e.g.*, extensibility of the language). This language is used to create applets. The aim of the study is to provide a formal description of a subset of the Clasp language and to use this description in order to prove properties. They prove by induction that certain run-time errors (*e.g.*, stack overflow, non-determinism) can never occur.

The Defensive Java Virtual Machine (dJVM) has been modelled using ACL2 [7]. This work aims to provide a JVM with run time checks in order to assure type-safe execution of the byte code. The only available document is a draft version where not all theorems were proved to our best knowledge. No information has been published on the complete proof of the model. An extension has been proposed [18] on verification related to proofs on object oriented byte code.

In [20], the authors propose a new approach to verify the properties of the Java Byte code using a model checker. A Java Card verifier performs an exhaustive search in the behavioural tree of the program in order to detect data flow or control flow errors. In fact, a byte code program can be seen as a description of the transition system. The state is given by the virtual machine state. Due to the potential infinite state of an arbitrary program, it is necessary to derive a finite abstraction of the program and to restrict as much as possible the usage of variables. This abstraction can be restricted to type information and the current method. The state is restricted to a method interpretation.

The INRIA proposes researches on the formal semantics of Java language; program analysis for program optimisation and methods for verifying safety and security related properties [11]. Most of the paper presented are more related with Java rather than Java card. The technique used for the verification of security properties is close to the previous one. They make an abstraction of the method under inspection. They translate it into a transition system and they verify some temporal formulae that describe an allowed path in the graph. Their transition graph is infinite but they proved that a bound exists on the state number. This allows them to use a model checker to verify their formulae [23]. In their model, all information related to the data flow were removed and only information linked with the control flow and the call graph of the program were kept. Some properties cannot be formalised with this approach like flow of classified information and detection of covert channel.

A recent paper [10] presents a model of the Windows for Smart Card runtime environment. The authors use the Abstract State Machine to describe formally their system. Gemplus provided several formal models of parts of the Java Card. We paid a particular attention to verify the correctness of the embedded code and to demonstrate the correctness of the JVM Firewall in [16], [17].

This intense activity about the formalisation of open operating systems from academic and industrial researchers points out the difficulty to be convinced by the soundness of the specification. There is currently an important effort in the Coq and Isabelle communities to completely formalise the Java semantics at the source and the byte code level. These efforts are supported by smart card manufacturers. The importance of the correctness of the byte code verifier requires a formalisation and the proof of this important piece of code. But unfortunately, this effort is far from the resource availability of each smart card manufacturer and will need some forms of collaboration between them. The complete proof of the verifier has been estimated at around 60 man/month.

Surprisingly, the B community has never paid a similar attention to the open operating system formalisation. In the Z community, we noticed only the work of the York University in collaboration with Logica. The smart card domain has several interesting and not confidential problems that can be solved using formal methods.

2.4 Reducing the cost of the test

We have seen that formal methods can be used for marketing motivation through the certification process and for security reason to ensure the soundness of the specification. The last point is related to productivity by reducing the cost of the test. Card manufacturers have a fairly extensive qualification process. Consequently, quality insurance requirements for smart cards are often very strong. In order to fulfil these requirements, card application providers have developed methods and tools adapted to smart card specific constraints. An important part of this development is devoted to test.

Starting from specifications, a tester enumerates all the tests that are necessary to verify that the product fulfils its requirements. It is then always possible to prove the conformity of the implementation regarding the specification. Moreover, this approach facilitates the maintenance of tests in case of product evolutions. In order to provide a high level of confidence, the testers use a data base which capitalizes all tests cases that can be done to reveal faults in smart card applications. Then, this approach takes advantages of fault driven testing approaches. The expected results of test are provided by a model of the application, which is developed in parallel with the product. At last, the test coverage can be estimated using a tool that evaluates the test coverage on the model. Test execution is fully automated. It is then possible to stress applications, in order to increase even more confidence on the application. This traditional approach has two major drawbacks: firstly, it needs to develop two instances of the program and any software evolution implies to modify the models, secondary during test execution if an error occurs (in fact a divergence in the behavior) both models must be checked. This process is secure but very costly. Generating the test cases automatically from a specification can reduce this process.

For generating test cases, we need a specification. Such specification can be obtained through a formal model. Some studies propose to generate the test cases from a B specification [1], [3]. During the last decade, testing theory and algorithms for the generation of tests have been developed from specifications modeled by variants of the Labeled Transition System model (LTS). A LTS is a structure consisting of states with transitions between them. Transitions are labeled with actions or events. The most efficient algorithms are based on adaptations of on-the-fly model-checking algorithms. Academic tools such as TGV [8] and now industrial tools such as TestComposer (Verilog) already exist. They implement these algorithms and produce correct test cases in a formal framework.

We choose to express the specification with an UML model. The specification is automatically translated into a labeled transition system thanks to the UMLAUT tool [12]. Then we use TGV to automatically produce test cases from this LTS and from test purposes produced by hand. We are now working on the methodology in order to help the applet designers to enrich the UML views in order to obtain a testable UML model.

3 The constraints

We have seen several good reasons of using formal specifications for smart card applications. Surprisingly, only the productivity advantage is well understood and accepted. Prior to integrate those methods in the development process, several points such as: development overhead, predictability, human resistance and tools must be solved. We believe that for the smart card domain, work must be done on the methodology, and tools must be improved in order to efficiently use formal methods.

3.1 Development overhead

We have to keep in mind that the smart card is a mass product and that its price must remain as low as possible in order to be competitive. The price of smart card ranges from 1 to 10 Euro depending on the chip and the gross profit is very weak. There is a strong pressure to reduce the development cost. The potential overhead introduced by formal methods remains acceptable under two conditions:

– If we develop generic components. For example, the backup mechanism, the memory anti-stress and the protocol layer are components that can be reused

in every smart card. This overhead is paid off on the number of produced smart cards.
– If we can reduce the test process. This can only be done if the development process is proven until the implementation. In this case it is possible to remove the unitary tests and save a lot of time. But unfortunately, the Atelier B is currently unable to generate the code that fit in the smart card. Moreover, when we proceed to an implementation a lot of restriction on the language are imposed. Several structures are not accepted in an IMPLEMENTATION clause.

Efficient conversion from specification to machine code is necessary for smart card based applications. In fact the current B0 translator has an overhead of more than 20% compared to a manually produced code [13]. If this overhead is acceptable for the code, it is too important for the RAM. For this purpose, we have developed a prototype of code translator in order to meet the smart card constraints [5].

3.2 Industrial constraints

Our main problem with a formal development is the lack of metrics to predict the duration of such a development. Predictability is of prime importance for smart card development, due to the burning phase. When a new development is scheduled, we have to keep a time slot to the chip manufacturer to burn the wafers (often a 10-14 months delay). This is often the critical path in the development process and it is very difficult to modify this time slot. For this reason, it is important to be able to meet the deadlines. Due to the lack of metrics, it remains very hazardous to evaluate the time needed for a new development. We have to improve our knowledge by developing several case studies in order to be able to give an accurate estimation. This allows to clearly identify the eventual caveats of the domain. For example, achieving the work described in [6] has proven useful when we decided to prove the FAÇADE verifier [9] even if the language and the static semantics are totally different the problem and the solutions where similar.

The second problem is the scalability. When we made our first model of the virtual machine with a reduced number of byte codes, the proof was easily manageable. Unfortunately, when we add new byte code, the complexity of the proof increased. This has been solved by a complete redesign of the formal specification. Solving a sub-problem cannot give accurate information of the complexity of the whole problem. The last point is more related with the tool. It is often better to adapt the design of the specification to the capacity of the prover by using the adequate structures.

For those reasons it is very difficult for a project manager to include formal methods in its product. We believe that the way to obtain their acceptance is to propose formal models for generic components and to develop higher level component (*e.g.*, a complete virtual machine) beside the development process.

3.3 Cultural resistance

One of the difficulties for a project manager to incorporate formal methods is the weight of the past. Until now, no bug has been discovered in a smart card. For smart card providers it seems natural to design secure system without formal methods. Moreover, formal methods cannot provide any help with the up-to-date attacks (Differential Power Analysis) against the smart card neither physical attacks. Logical attacks are often less considered but this idea must be left out when considering open operating systems.

Another point is related to the designer. It is difficult to express an abstraction of a problem and to refine it. People are considering formal language like B as a new programming language and they have a lot of difficulties (abstraction capabilities, less expressive language). This point can be solved by adequate training but if remains difficult to specify a provable model.

3.4 Need of a methodology

We believe that a clean methodology with related metrics and tools improvements would consequently help the integration of formal methods and in particular B in the software process. It is important to have guidelines for the specifications and proofs that help the designers. For this purpose we joined a European project, named MATISSE in collaboration with MATRA, Soton university, Abo Akademi, Steria and DERA. In this project we will exploit and enhance existing methodologies and associated technologies that support the correct construction of critical systems.

Our own methodology is related to the certification process. It's often said that the use of formal methods is time consuming and very costly, they required very skilled people and there is an important gap between the semi formal and the formal specification. But combining a semi formal language like UML and a formal method like B is probably the less expensive way to reach the CC requirements. In [17], we explain how to apply this methodology for a smart card certification. But if this approach is well suited for certification it does not help a lot for modelling a system. Some work have been done in this direction [19] for translating UML views, but our own experience shows the difficulty to match a B model to an UML class diagram. Even if B shares some characteristics with object languages, the B architecture clauses have not the same expressiveness. We prefer to have two approaches: one dedicated to certification with a preliminary semi formal work, and a second one with a preliminary informal work: rewriting the specifications in order to clarify them.

The lack of metrics for a B development is a problem either for predictability and quality measurement. It is often said that a high ratio of automatically proved proof obligations (PO) is an indication of a good design. Unfortunately, our own experience shows that sometimes this indicator is wrong. For example, we made two models of a virtual machine, one naïve but we a high ratio of automatically proven PO and a second one where we regrouped the opcode per properties. In the latter case, the ratio was poor (around 40%) but the proofs were generic [21]. And the complete proof of the specification has been done with the second model in a shorter time. We expect that MATISSE will reveal some metrics for quality assessment.

We expect also some tool improvements. The first one is linked to the code generator that must be considerably improved in order to generate code that fits the smart card constraints. But other points must also be improved from ergonomics to proof management. The proof tree is unusable in the current version of the tool, it is impossible to explicitly name the hypothesis, any modification of the specification and the proof can be lost. There are no proof editor, neither any means to eliminate unusable hypotheses in the stack. Currently a lot of academic work are done around the tools for the B method (parser, test generator, code generator) and the recent announcement of Steria about the GPL licence of the B compiler will probably help to the tool improvement.

4 Conclusions

Smart Card domain is not yet the expected success story but is probably the ideal field for applying formal methods. There are a lot of good reasons for formal methods to be well accepted. One way to differentiate card manufacturers will be on security aspect and the relevant method to reach it. This goal can be achieved through the certification process that is now well handled for the medium level (*e.g.*, EAL5). But a new effort must be set up in order to reach the higher levels. Certification is only the visible part of the iceberg. The security of smart cards relies on other work that are probably more fruitful for example the generic components of the smart cards. But in order to generalize the use of formal methods, we have to prepare their integration in the software process, which remains the real challenge. For achieving it, a lot of work must be done on the methodology, the associated metrics and on the tools.

We believe that there is not only one formal method that is suitable for smart cards. The success of the PACAP project [4] and the well acceptance of the test generation clearly show that there is enough room for different methods. We have now to define the adequate form (size, training, and mission) for a formal method team developing models for the Gemplus R&D.

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